

REMARKS/ARGUMENTS

In this amendment, no claims are amended, canceled, or added. Thus, claims 1-23 remain pending.

Rejection under 35 U.S.C. § 103, Diamant in view of Benson

Claims 1-6, 13-15, 18, 19, and 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant (U.S. Patent Publication No. 200410122997) in view of Benson et al. ("Benson") (U.S. Patent No. 5,542,076).

Claims 1-13

Claim 1 is allowable over Diamant and Benson, either alone or in combination, as those references fail to disclose or suggest all the elements of claim 1. For example, claim 1 recites:

in response to a detected interrupt, determining whether the detected interrupt was generated by one of the plurality of co-processors of the multiprocessor subsystem; and

in the event that the detected interrupt was generated by one of the plurality of co-processors, scheduling execution of a deferred servicing procedure,

wherein during execution the deferred servicing procedure services a plurality of pending interrupts generated by two or more of the plurality of co-processors, including the detected interrupt.

Time periods of Benson are not scheduled in the event of a detected interrupt

In the Response to Arguments (paragraph 9), the Office Action states that "the servicing of interrupts that only arrive within the predetermined time period is considered equivalent to the 'deferred servicing procedure,'" as recited in claim 1. It is a little unclear to which predetermined time period that is being referred. There are two predetermined time periods discussed in Benson.

The first predetermined time period is Toff, which is implemented as follows. *See Benson*, Figure 3. "As long as Nc, represented by the number in interrupt counter 160, is less than the threshold value THLD, controller 30 continues to process the interrupts." *Id.*, col. 5 lines 64-66. When Nc "becomes greater than the threshold value THLD, the interrupt service is

disabled for a predetermined period of time, denoted as Toff in FIG. 3." *Id.*, col. 6 lines 1-3 (emphasis added). As there are no interrupts that are serviced during the time period Toff, then Toff cannot be the deferred servicing procedure of claim 1.

The other predetermined time is the time period T of Figure 4. At the beginning of each time period T, interrupt servicing is enabled. *Id.*, col. 6 lines 25-26. Once an interrupt is received, interrupts are disabled in step 300, and the received interrupt is serviced at step 320 in the known manner. *Id.*, col. 6 lines 33-43. If CNT becomes greater than the threshold value THLD in the threshold register 180, then servicing interrupts is disabled for the rest of the period T so that controller 30 can do other work. *Id.*, col. 6 lines 46-57.

The time period T is started upon a leading edge of a square wave that is part of a clock signal CLK generated by a timer 200. *Id.*, col. 5 lines 39-41. Thus, the time period T is started based on a clock signal and not in response to or in the event of a detected interrupt. Accordingly, even if the predetermined time period T could be equated with a deferred servicing procedure, the time period T is not scheduled "*in the event that the detected interrupt was generated by one of the plurality of co-processors,*" as recited in claim 1.

Combination of Benson with Diamant does not change behavior of predetermined time periods

Both Diamant and Benson start the individual servicing of interrupts based on an interrupt signal. *See Benson*, col. 4 lines 53-55; *See Diamant*, paragraphs 41 and 42. Benson is directed to limiting the individual servicing procedures based on the time period T as discussed above. Thus, the combination would use the time period mechanism of Benson to stop the individual servicing procedures of Diamant to alleviate problems of too many interrupts being serviced within the time period T. As noted above, the time period T does not teach or suggest a deferred servicing procedure scheduled "*in the event that the detected interrupt was generated by one of the plurality of co-processors,*" as recited in claim 1.

Accordingly, the combination does not teach or suggest one deferred servicing procedure such that satisfies both limitations of "*in the event that the detected interrupt was generated by one of the plurality of co-processors, scheduling execution of a deferred servicing procedure*" and "*wherein during execution the deferred servicing procedure services a plurality*

of pending interrupts generated by two or more of the plurality of co-processors, including the detected interrupt," as recited in claim 1.

For at least these reasons, claim 1 is allowable over Diamant in view of Benson. As claim 1 is allowable, dependent claims 2-13 and 22-23 are also allowable for at least the same rationale.

Other Rejections under 35 U.S.C. § 103

Claims 10-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant in view of Benson as applied to claim 1 above (hereinafter "Diamant- Benson"), and further in view of Simpson (U.S. Patent No. 5,867,687). Claims 10-12, which depend upon claim 1, and claim 17, which depends upon claim 14, are allowable for at least the same rationale as claim 1.

Simpson is cited as teaching the handling interrupts based on multiple priority levels. (Office Action page 7). Even assuming that Simpson teaches this limitation and that there is a motivation to combine, this teaching does not make up for the deficiencies in the other references with respect to these claims.

Claims 8, 16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant-Benson in view of Alasti et al. ("Alasti") (U.S. Patent No. 6,574,693). Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant- Benson in view of Alasti as applied to claim 8 above (hereinafter "DBA"), and further in view of Simpson.

Claims 8 and 9 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claims 16 and 22 depend upon claim 14 and is allowable for at least the same rationale as claim 14.

Alasti is directed to the disabling of interrupts from certain subsystems, such as power management, when a processor is within a certain context. *See Alasti*, abstract line 8 and page 5 line 63. Even assuming that this aspect of Alasti teaches disabling interrupts from co-processors of a subsystem in the event of a detected interrupt being generated by one of the co-processors of the subsystem and that there is a motivation to combine with Simpson, Diamant

and Benson, this teaching does not make up for the deficiencies in these references with respect to these claims.

Objection to Claims 7 and 20

Claims 7 and 20 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form. In view of the foregoing arguments with regard to claims 1 and 14, Applicant respectfully submits that claims 7 and 20 are in condition for allowance without being rewritten in independent form. Withdrawal of the objection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

/David B. Raczkowski/

David B. Raczkowski
Reg. No. 52,145

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
DBR:lrj
61105601 v1